IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-9 (cancelled)

Claim 10 (original) A processing system comprising:

a first branch history table comprising a plurality of bimodally accessed entries for storing a first set of branch prediction bits;

a second branch history table comprising a plurality of fetch-based accessed entries for storing a second set of branch prediction bits;

a selector for selecting in response to a selection control bit selected from a set of selection control bits, a bit from a selected one of said sets of bits accessed from said first and second branch history tables; and

a selector table comprising a plurality of entries for storing said a set of selector bits as a function of a performance history of said first and second sets of branch prediction bits stored in said first and second branch history tables, wherein said each said entry in said tables comprises a 1-bit counter.

Claims 11-20 (cancelled)

Claim 21 (currently amended) Branch prediction circuitry comprising:

a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address;

a fetch-based branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of said branch address and bits from a history register, each entry of the fetch-based branch history table operable for containing bits representing a prediction value for a plurality of branches in a fetch group, wherein each fetch group is represented by a bit in the history register; and

a selector table comprising a plurality of entries each for storing a plurality of selection bits and accessed by a pointer generated from selected bits from said branch address and bits from said history register, each said selector bit used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from said fetch-based history table.

Claim 22 (previously presented) The branch prediction circuitry of Claim 21 and further comprising circuitry for updating said bimodal and fetch-based branch history tables operable to:

set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time; and

set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time.

Claim 23 (previously presented) The branch prediction circuitry of Claim 21 wherein said history register comprises a shift register and said branch prediction circuitry further comprises circuitry for updating said shift register by shifting in a preselected prediction value for each fetch group.

Claim 24 (previously presented) The branch prediction circuitry of Claim 21 and further comprising circuitry for updating said selector table operable to:

update a corresponding bit in a selected entry in said selector table with a first value when a bimodal prediction value from said bimodal branch history table correctly represents a corresponding branch resolution; and

update a corresponding bit in a selected entry in said selector table with a second value when a fetch-based prediction value from said fetch-based branch history table correctly represents the corresponding branch resolution.

Claim 25 (previously presented) The branch prediction circuitry of Claim 21 wherein the plurality of selection bits are operable for selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table.

Claim 26 (previously presented) The branch prediction circuitry of Claim 23 wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when corresponding values from said bimodal and fetch-based branch history tables both correctly represent a corresponding branch resolution, and wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when neither values from said bimodal and fetch-based branch history tables correctly represent a corresponding branch resolution.

Claim 27 (previously presented) The branch prediction circuitry of Claim 23 wherein said circuitry for updating said selector table is further operable to set a value in a selected entry in said selector table to a value associated with said fetch-based table when corresponding values from said bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome.

Claim 28 (previously presented) A processing system comprising:

a first branch history table comprising a plurality of bimodally accessed entries, each entry for storing a first set of branch prediction bits;

a second branch history table comprising a plurality of fetch-based accessed entries each entry for storing a second set of branch prediction bits;

a selector for selecting, in response to a plurality of selection control bits, a set of prediction bits from a selected one of said sets of bits accessed from said first and second branch history tables; and

a selector table comprising a plurality of entries, each entry for storing a plurality of selection control bits wherein the selection control bits are set as a function of a performance history of corresponding first and second sets of branch prediction bits stored in said first and second branch history tables.

Claim 29 (previously presented) The processing system of Claim 28 wherein said entries of said selector table are accessed using fetch-based accessing.

Claim 30 (previously presented) The processing system of Claim 28 wherein said each said entry in said tables comprises a 1-bit counter.

Claim 31 (previously presented) The processing system of Claim 28 wherein said first and second branch history tables and said selector table form a portion of a branch execution unit.

Claim 32 (previously presented) The processing system of Claim 31 wherein said branch execution unit forms a part of a microprocessor.

Claim 33 (previously presented) The processing system of Claim 32 and further comprising memory coupled to said microprocessor.

Claim 34 (previously presented) A method of performing branch predictions in a processing system including a bimodal branch history table, a fetch-based branch history table and a selector table, the method comprising the substeps of:

accessing the bimodal branch history table to retrieve a first set of branch prediction bits;

accessing the fetch-based branch history table to retrieve a set of second branch prediction bits;

selecting between the first and second sets of branch prediction bits in response to corresponding bits retrieved from the selector table, wherein a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits is not less than a number of instructions in a fetch group; and

updating the selector table as a function of actual branch resolution.

Claim 35 (previously presented) The method of Claim 34 wherein said step of updating the selector table comprises the substeps of:

determining if at least one of the first set of branch prediction bits correctly predicts the corresponding branch resolution outcome;

updating the corresponding entry in the selector table to a first logic value when the at least one of the first set of prediction bits correctly represents the branch resolution outcome;

determining if at least one of the second set of branch prediction bits correctly predicts the branch resolution outcome; and

updating the corresponding entry in the selector table to a second logic value when the at least one of the second set of branch prediction bits correctly represents the branch resolution outcome.

Claim 36 (previously presented) The method of Claim 35 and further comprising the steps of:

determining if at least one bit of both the first and second sets of branch history bits correctly predict the branch resolution outcome;

maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome;

determining if at least one bit of both the first and second sets of branch prediction bits incorrectly predict the branch resolution outcome; and

maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch history bits incorrectly predict the branch history outcome.

Claim 37 (previously presented) The method of Claim 35 and further comprising the steps of :

determining whether at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome;

maintaining the current value of corresponding bits in the corresponding selector table entry when at the least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome; and

updating the current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome.

Claim 38 (previously presented) The method of Claim 34 wherein said step of accessing the fetch-based branch history table comprises the substep of generating an address from at least some bits of a branching instruction and bits retrieved from a history register.

Claim 39 (previously presented) The method of Claim 38 wherein the history register comprises a shift register.

Claim 40 (previously presented) The method of Claim 39 wherein said method further comprises the steps of updating the shift register by shifting in a prediction bit for each fetch group.

Respectfully submitted,

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